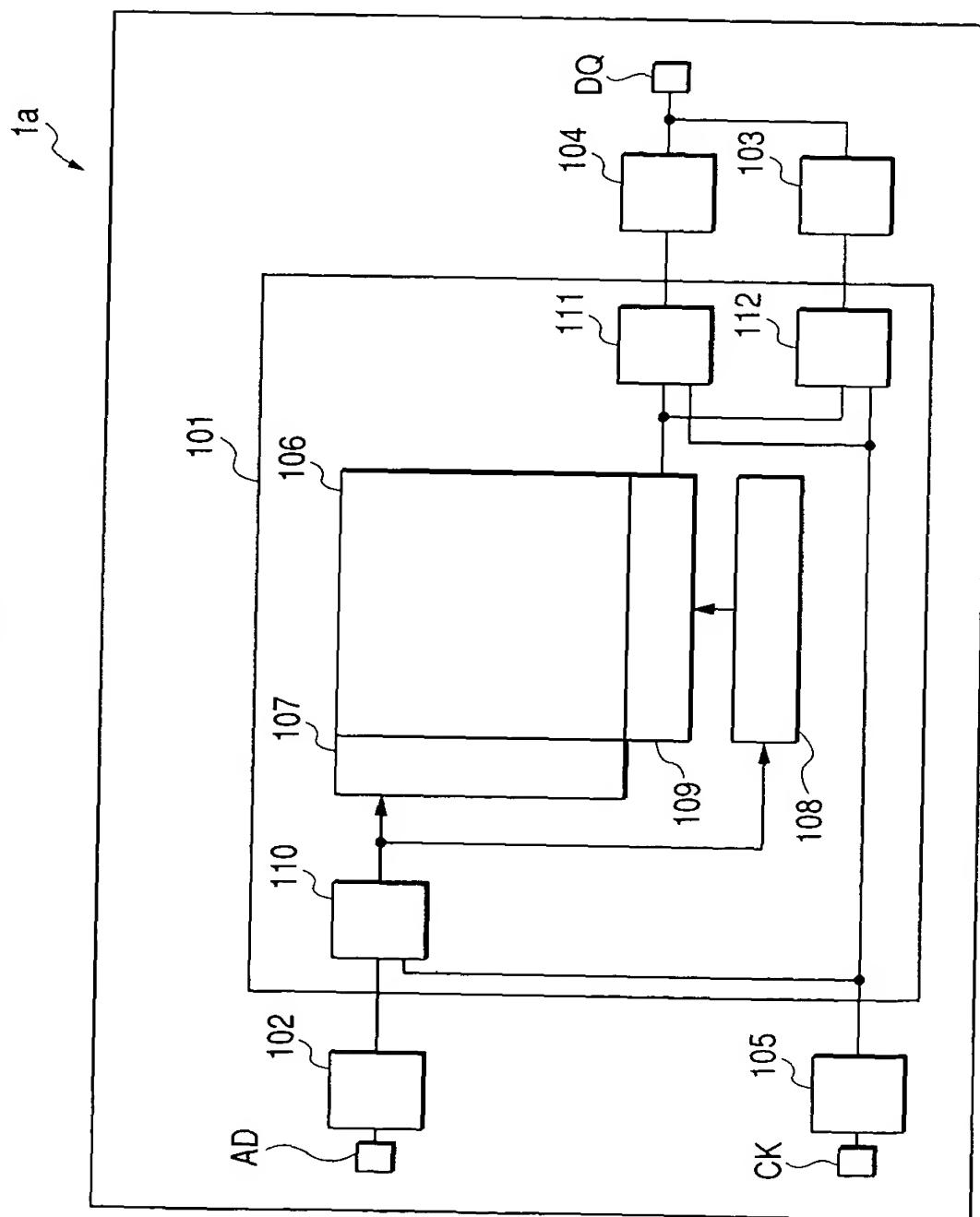


APPROVED BY DRAFTSMAN	O.G. FIG. CLASS	SUBCLASS
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1 / 30

FIG. 1

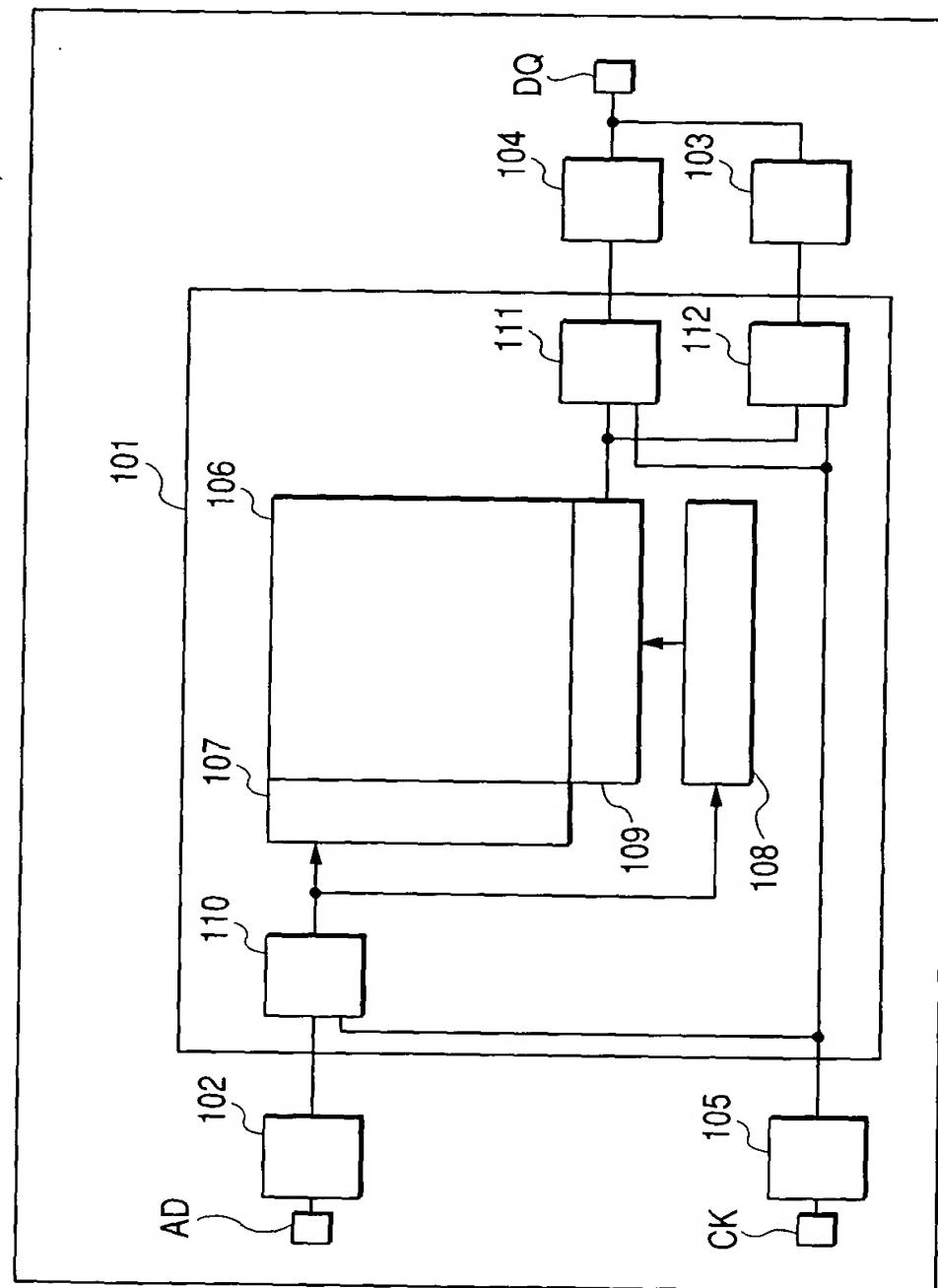


APPROVED	O.G. FIG.
BY	CLASS SUBCLASS
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FIG. 2

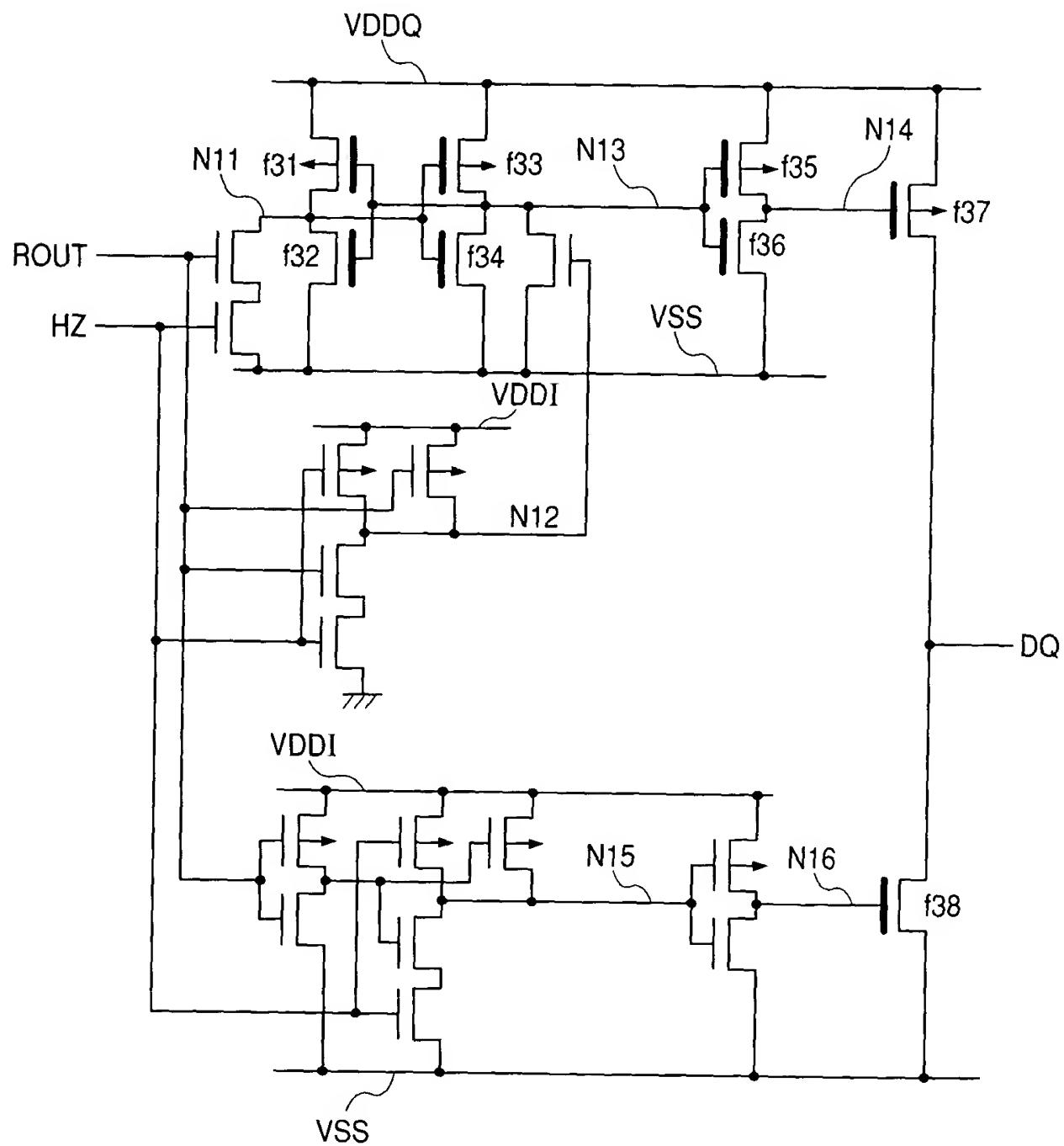
1b



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FIG. 3

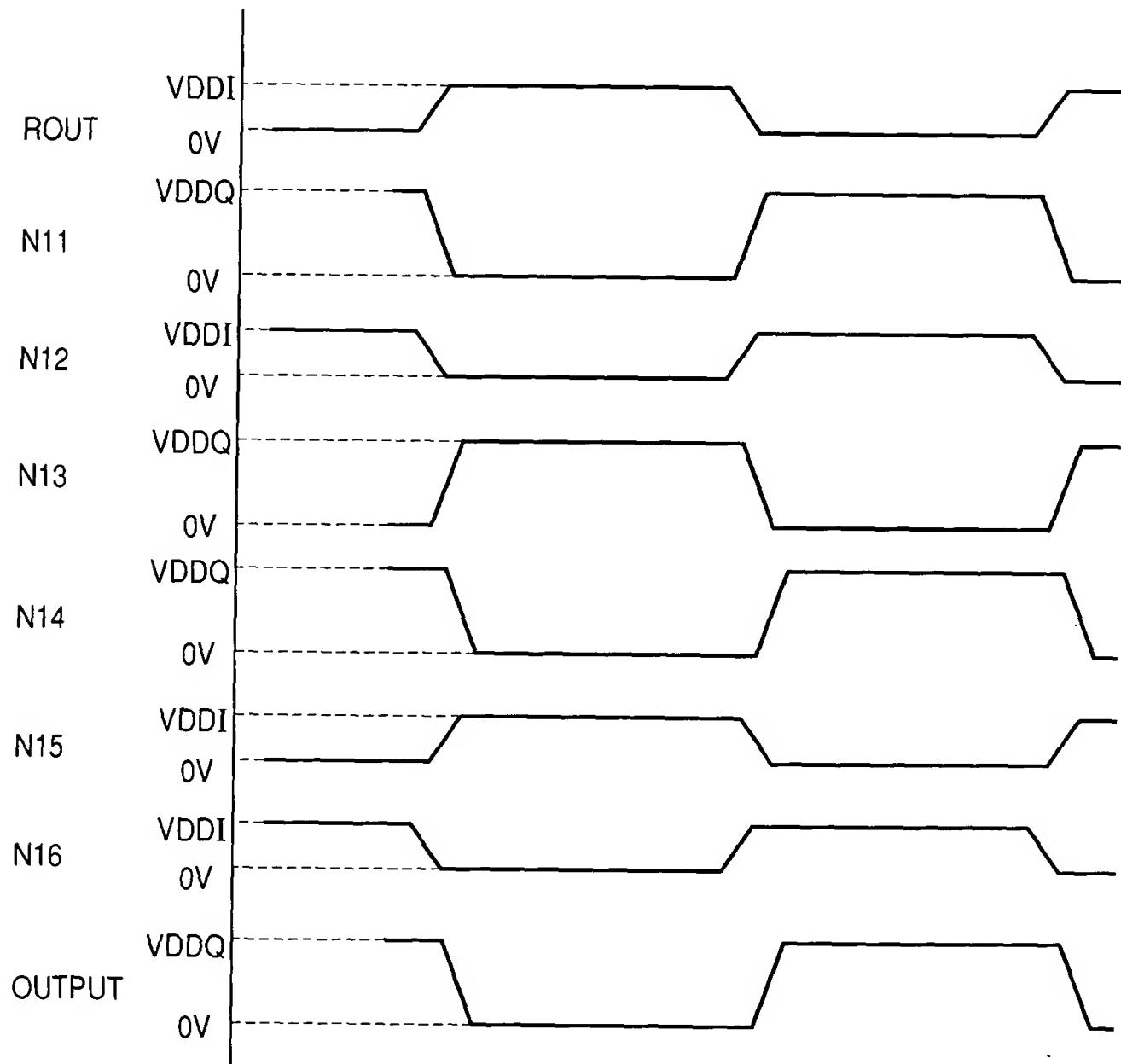


APPROVED	O.G. FIG.
BY	CLASS SUBCLASS
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FIG. 4

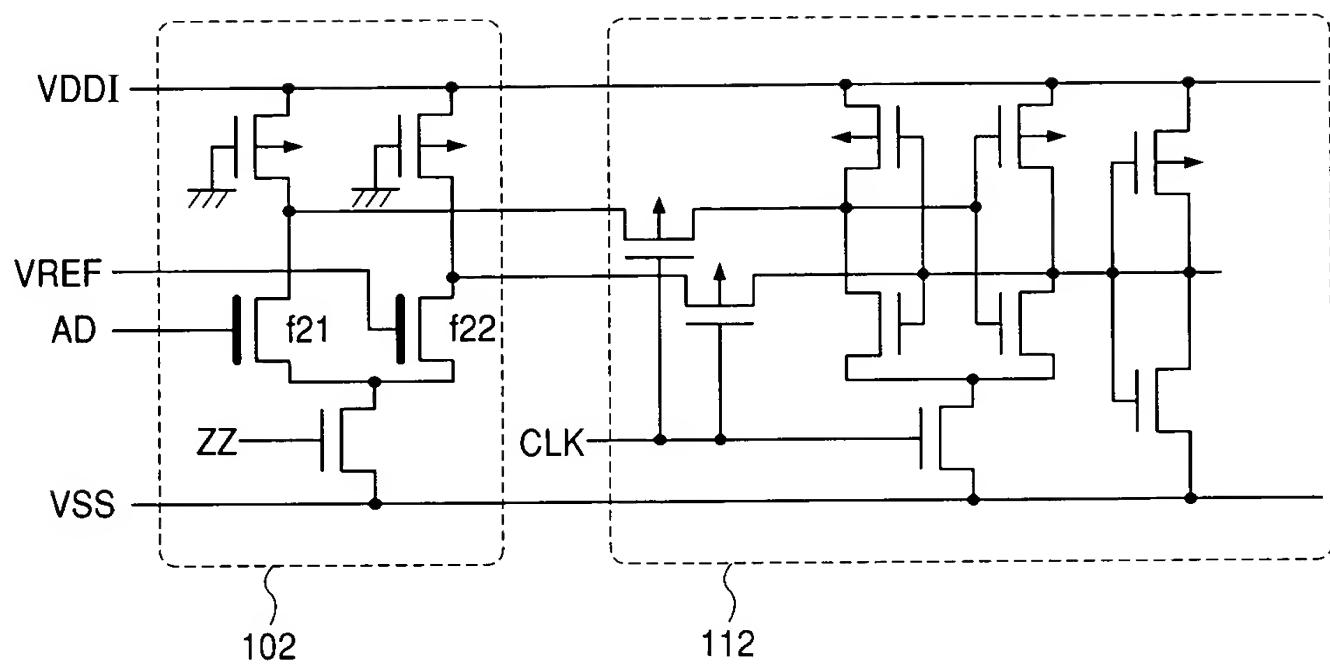
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DRAFTSMAN	SUBCLASS

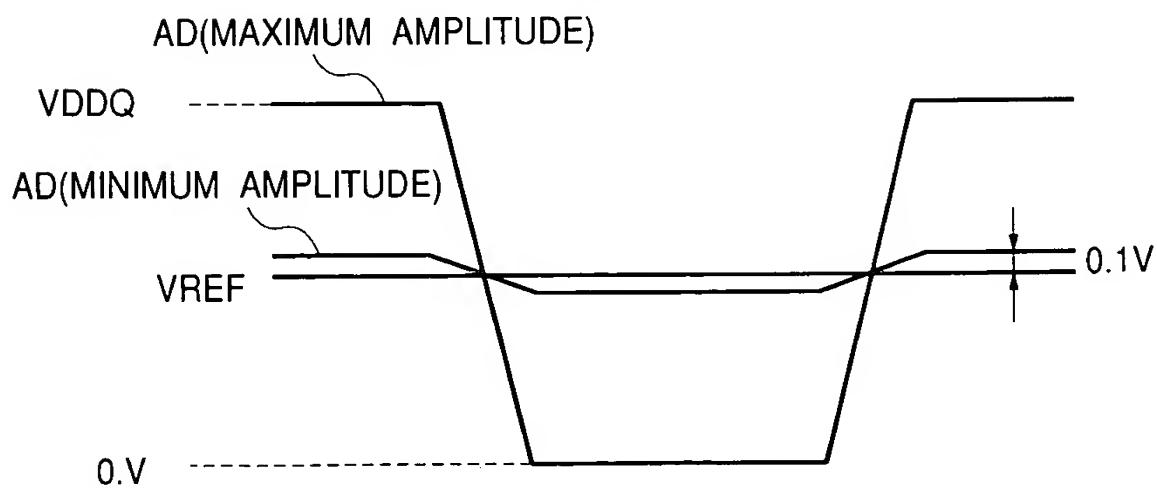
5 / 30

FIG. 5



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FIG. 6



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	CLASS
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FIG. 7(a)

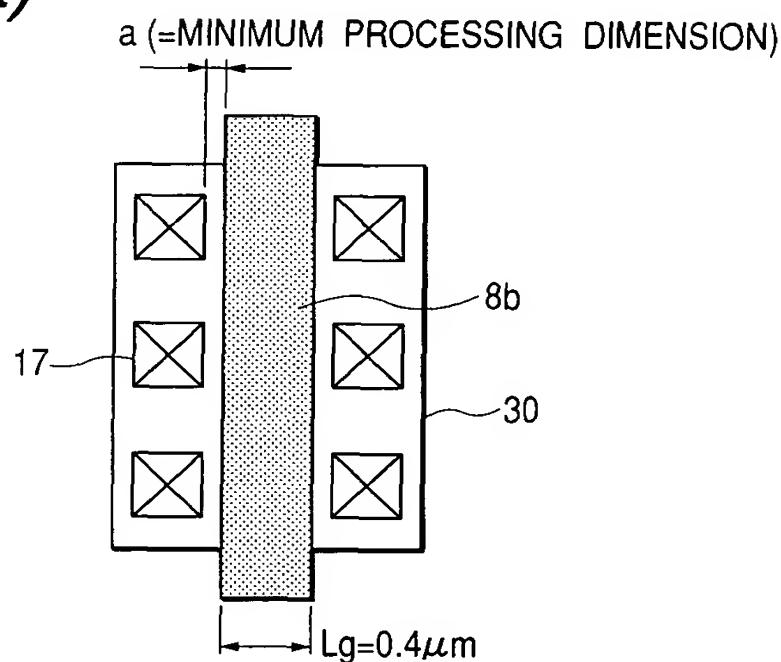
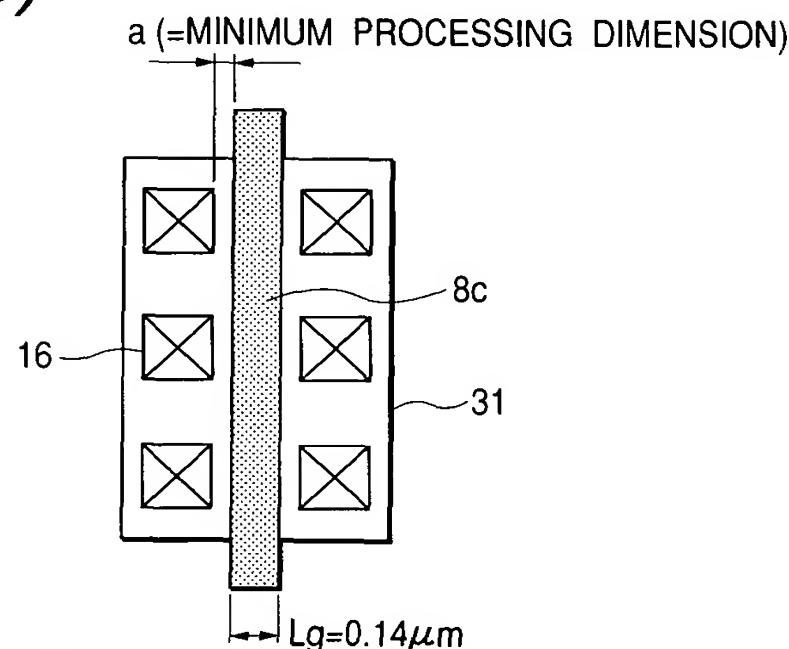


FIG. 7(b)

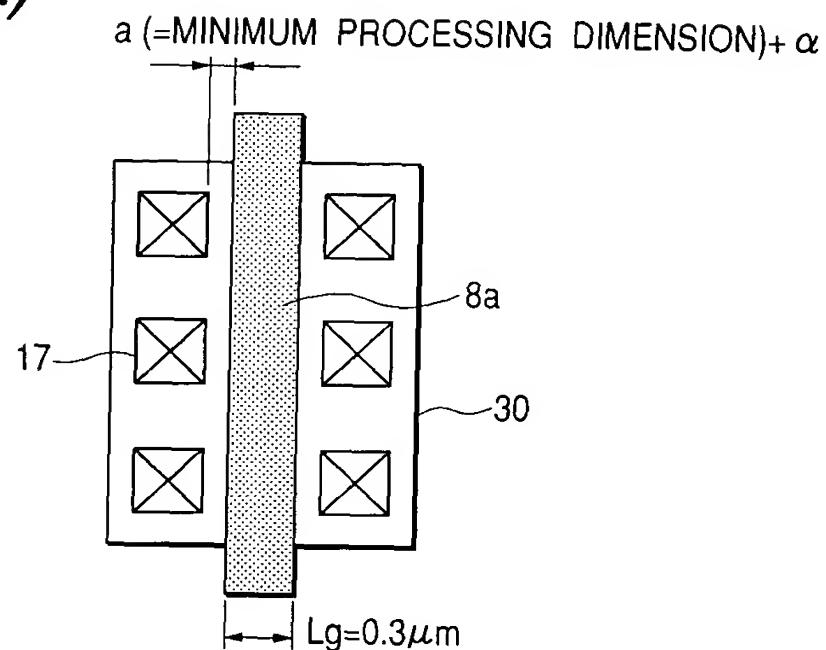


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APPROVED	O.G. FIG.
BY	CLASS SUBCLASS
DRAFTSMAN	

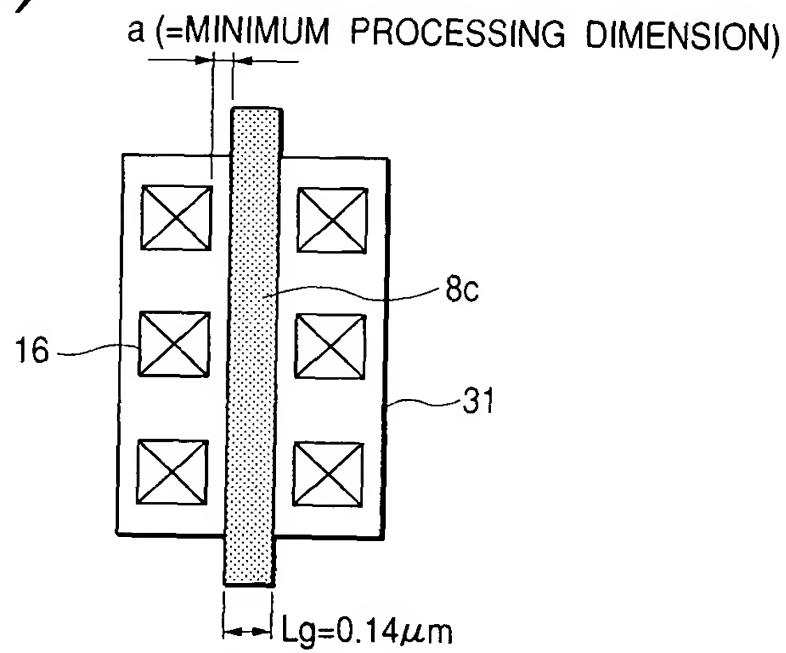
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FIG. 8(a)



2.5V WITHSTANDING MOS TRANSISTOR

FIG. 8(b)



1.5V WITHSTANDING MOS TRANSISTOR

APPROVED BY	O.G. FIG.
DRAFTSMAN	CLASS SUBCLASS

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FIG. 9

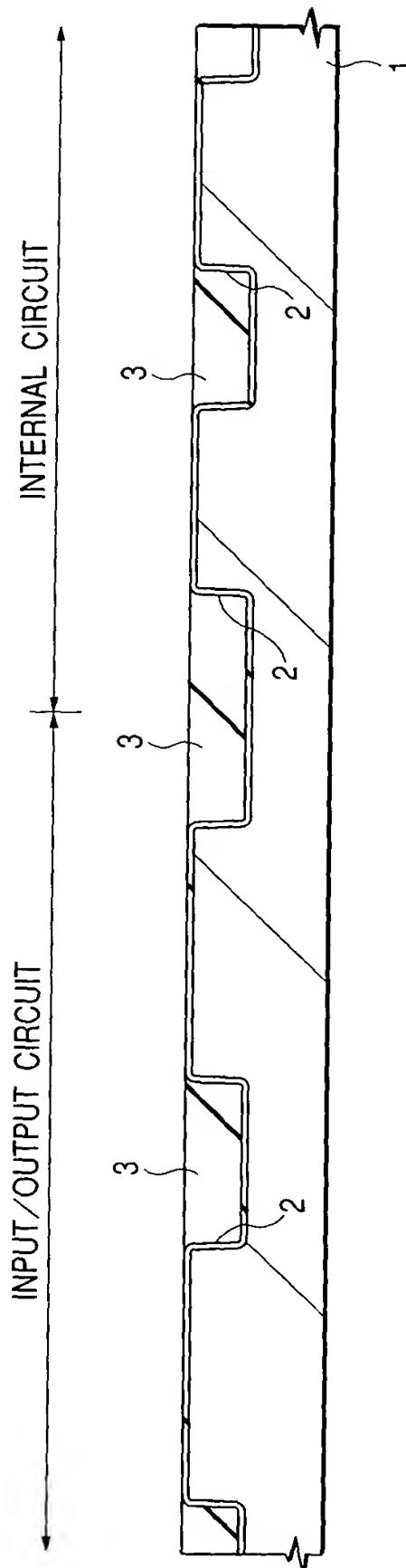
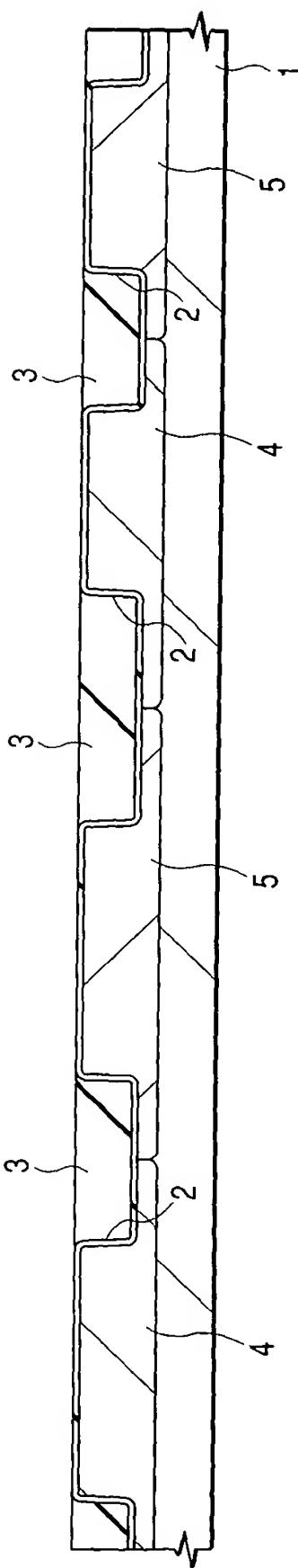


FIG. 10



APPROVED	O.G. FIG.
BY	CLASS / SUBCLAS
DRAFTSMAN	

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FIG. 11(a)

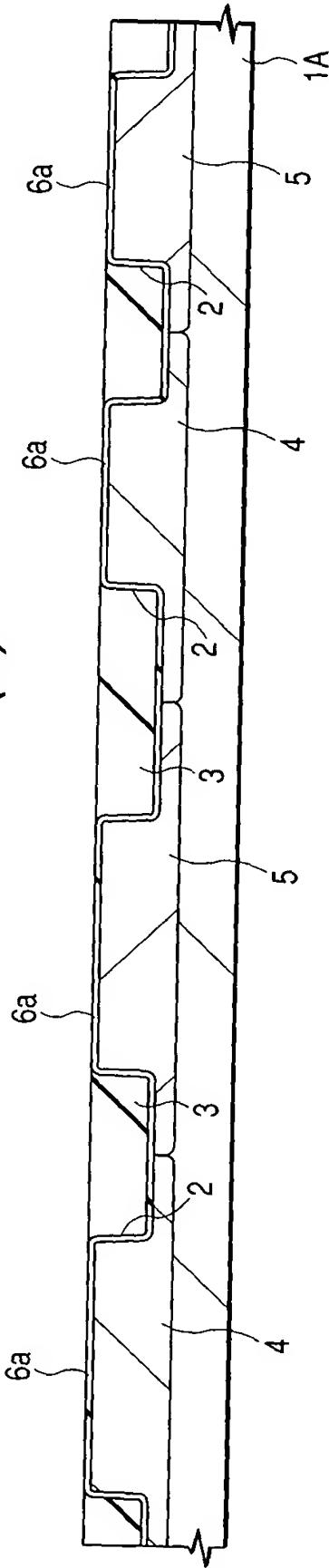
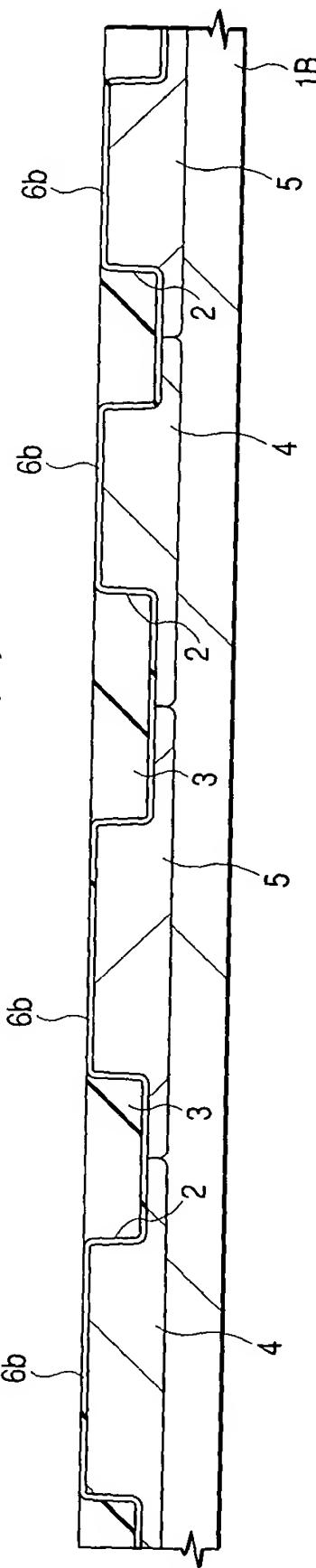


FIG. 11(b)



APPROVED	O.G. FIG.
BY	CLASS SUBCLASS
DRAFTSMAN	

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FIG. 12(a)

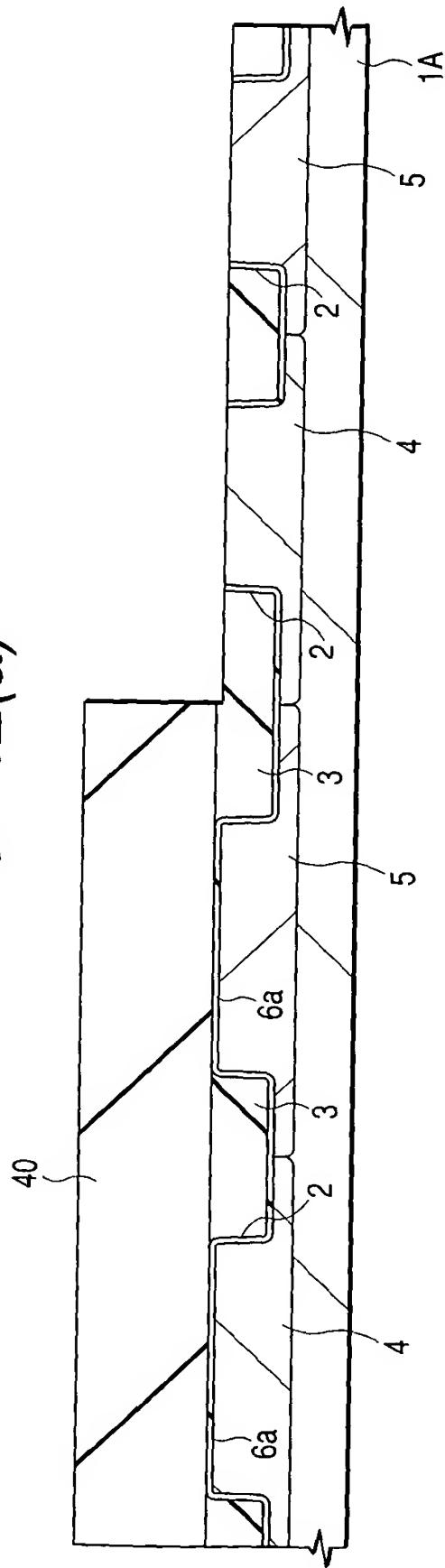
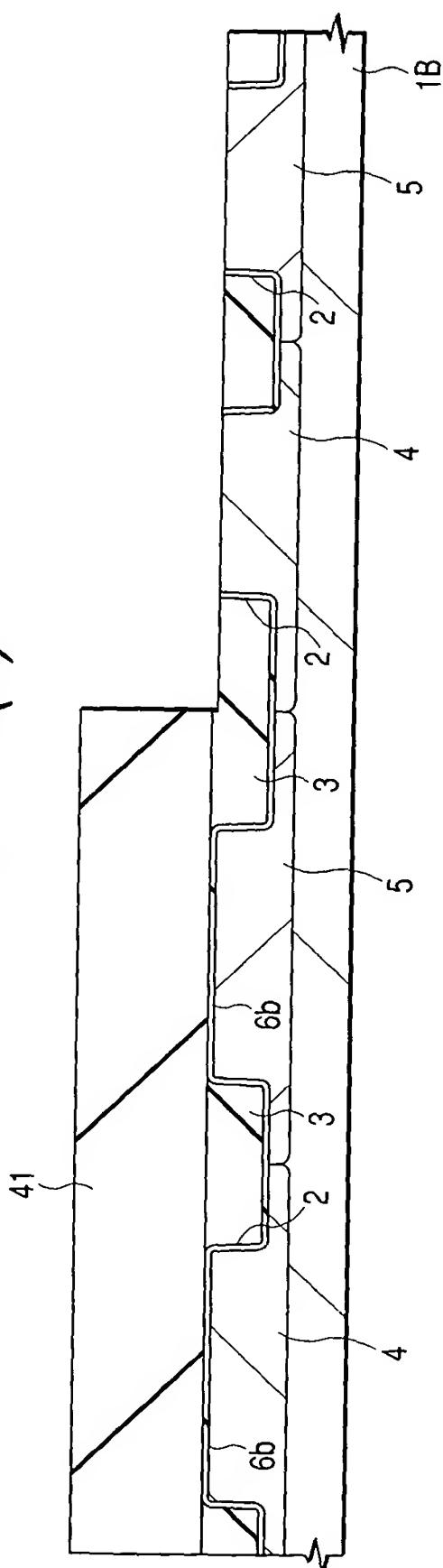


FIG. 12(b)



APPROVED	O.G. FIG.
BY	CLASS SUBCLASS
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FIG. 13(a)

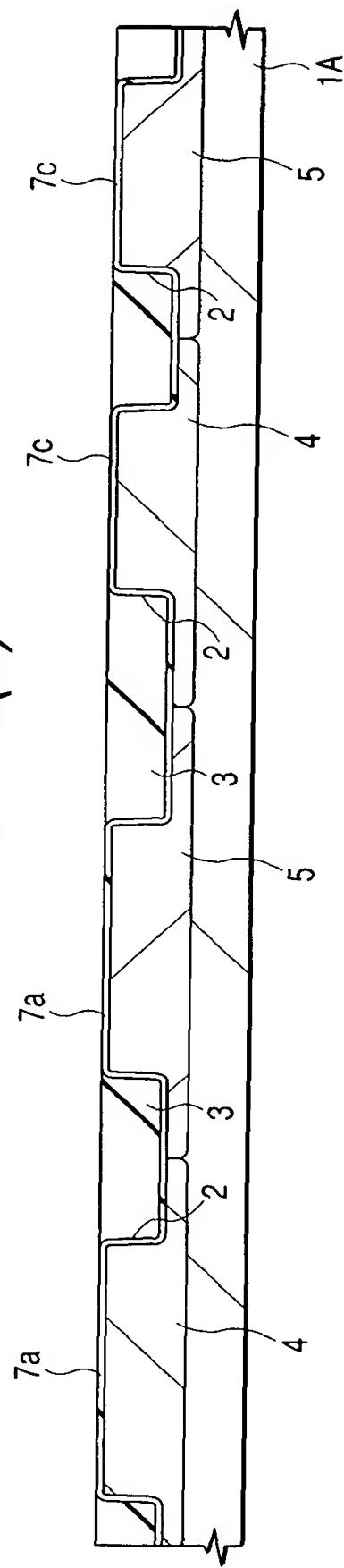
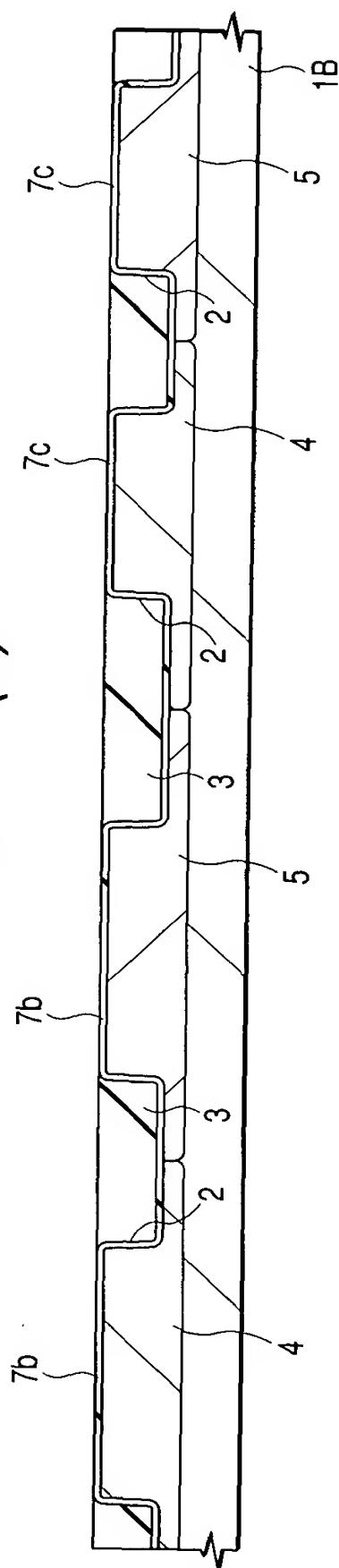


FIG. 13(b)



APPROVED	O.G. FIG.
BY	CLASS SUBCLASS
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FIG. 14(a)

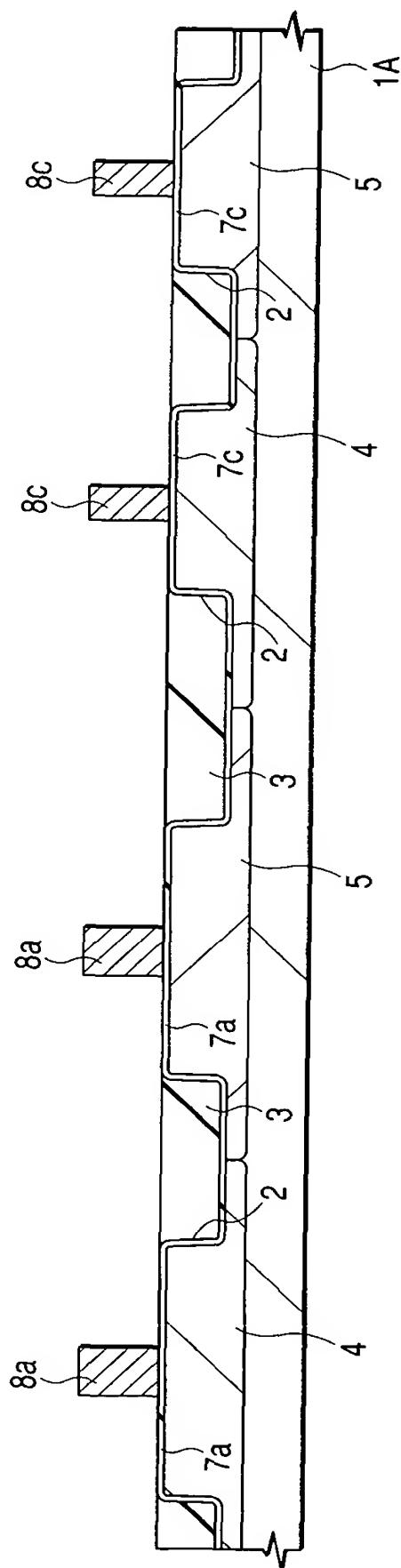
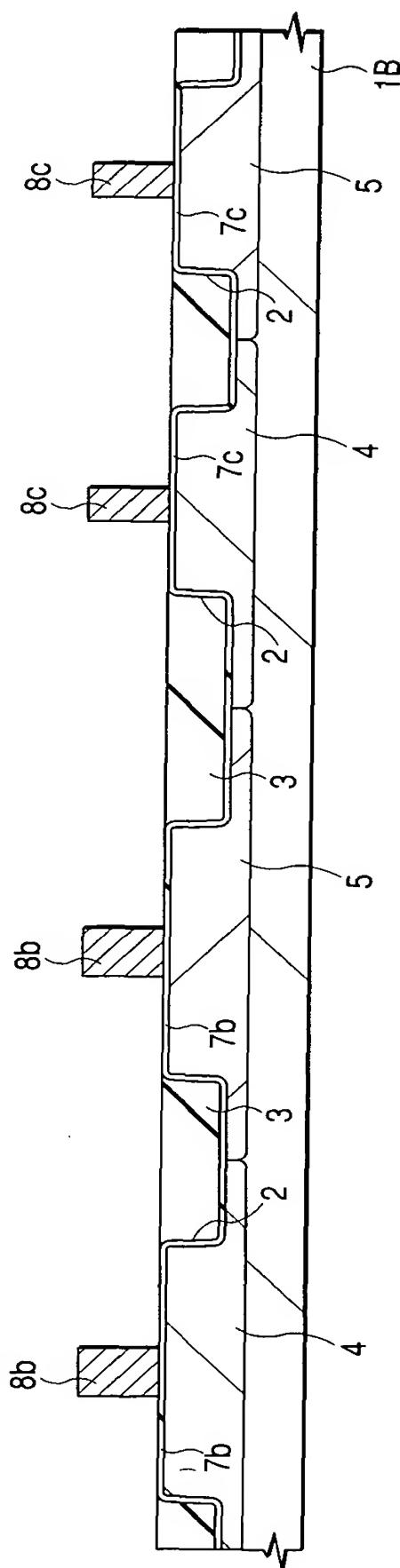


FIG. 14(b)



APPROVED	O.G. FIG.
BY	CLASS SUBCLASS
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FIG. 15(a)

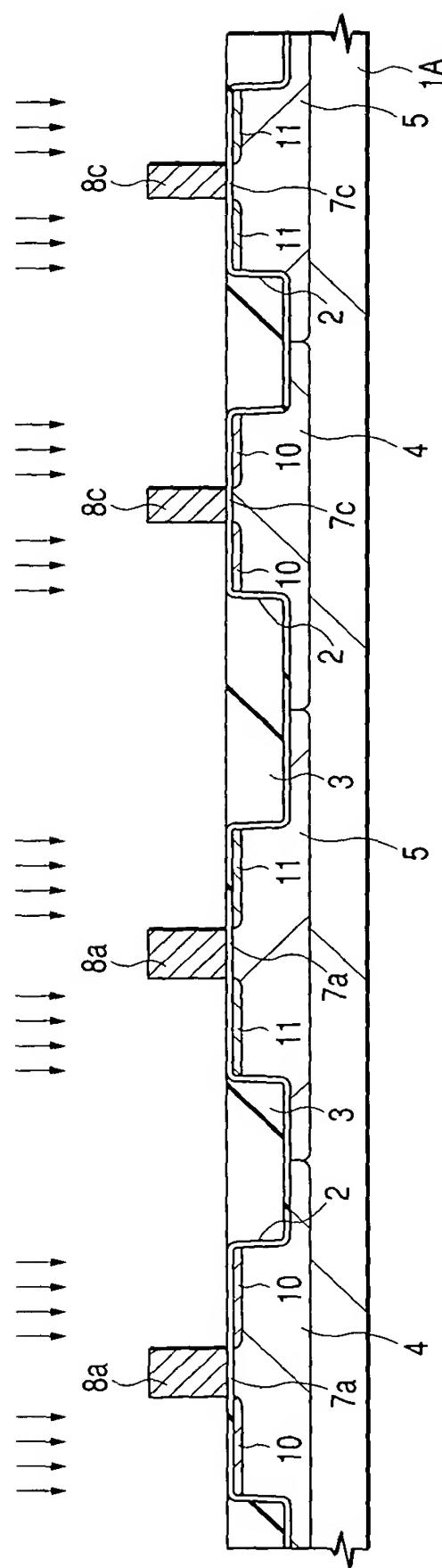


FIG. 15(b)

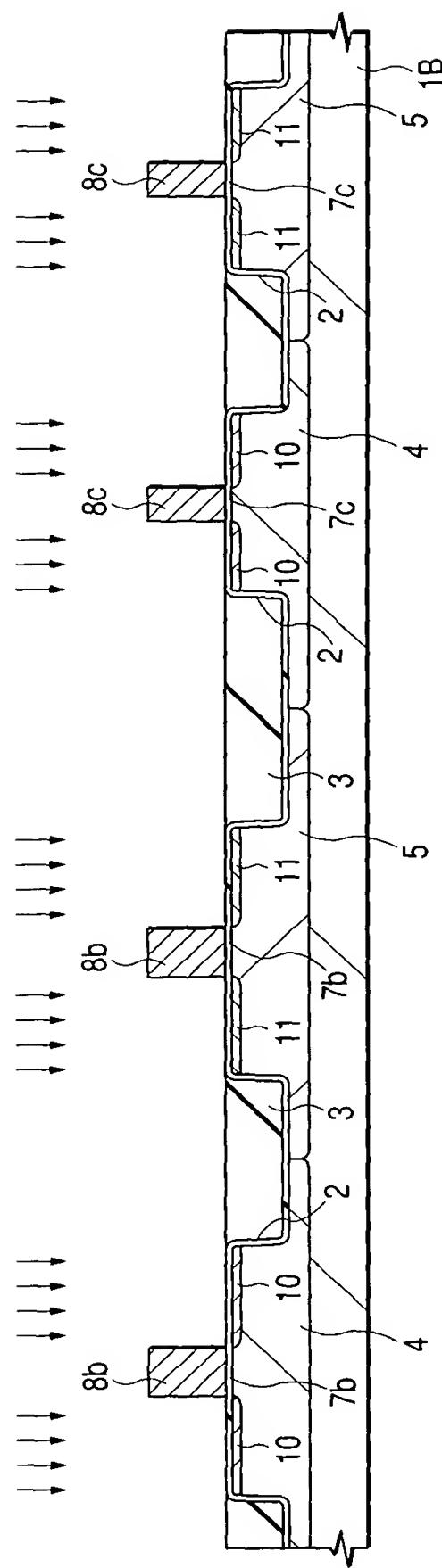


FIG. 16(a)

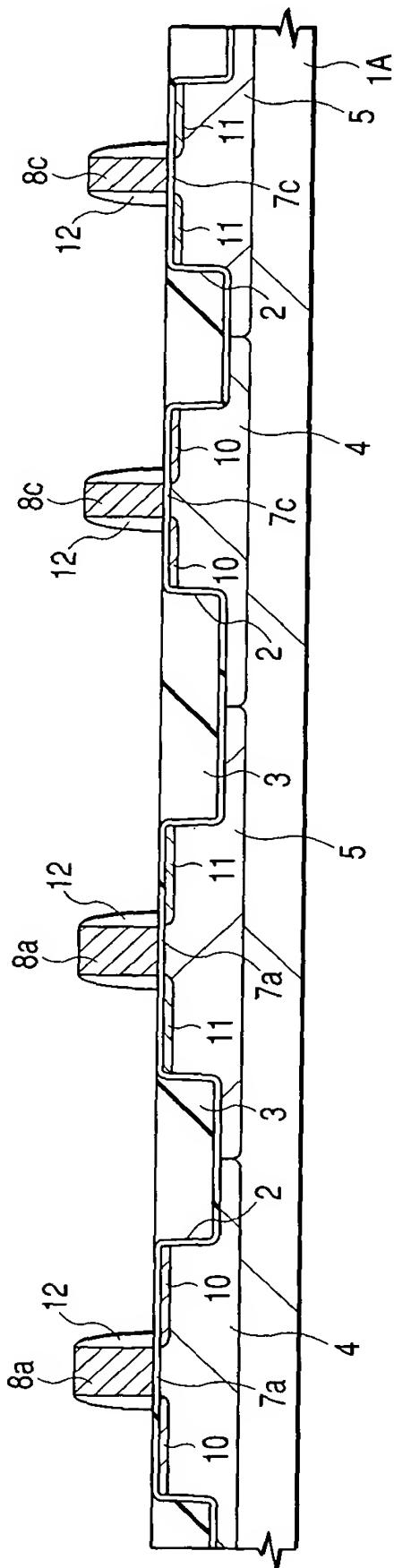
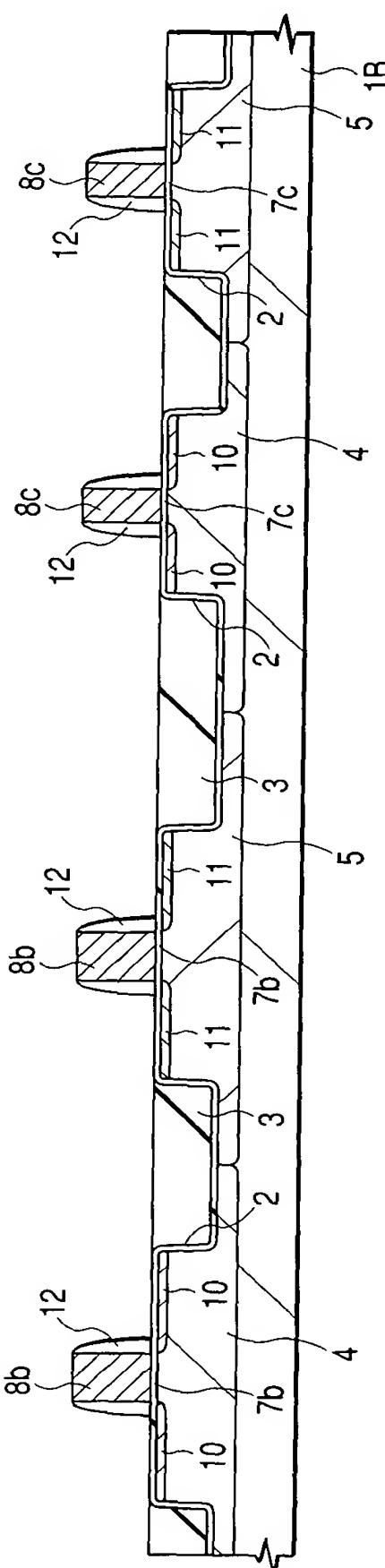


FIG. 16(b)



APPROVED	O.G. FIG.
BY	CLASS SUBCLASS
DRAFTSMAN	

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FIG. 17(a)

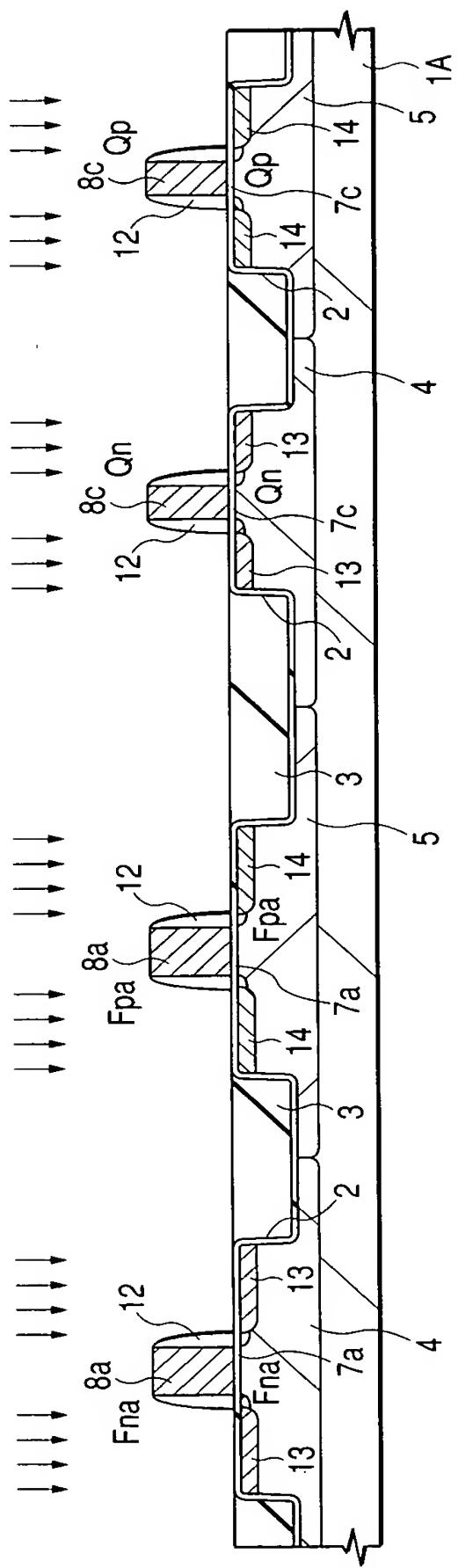
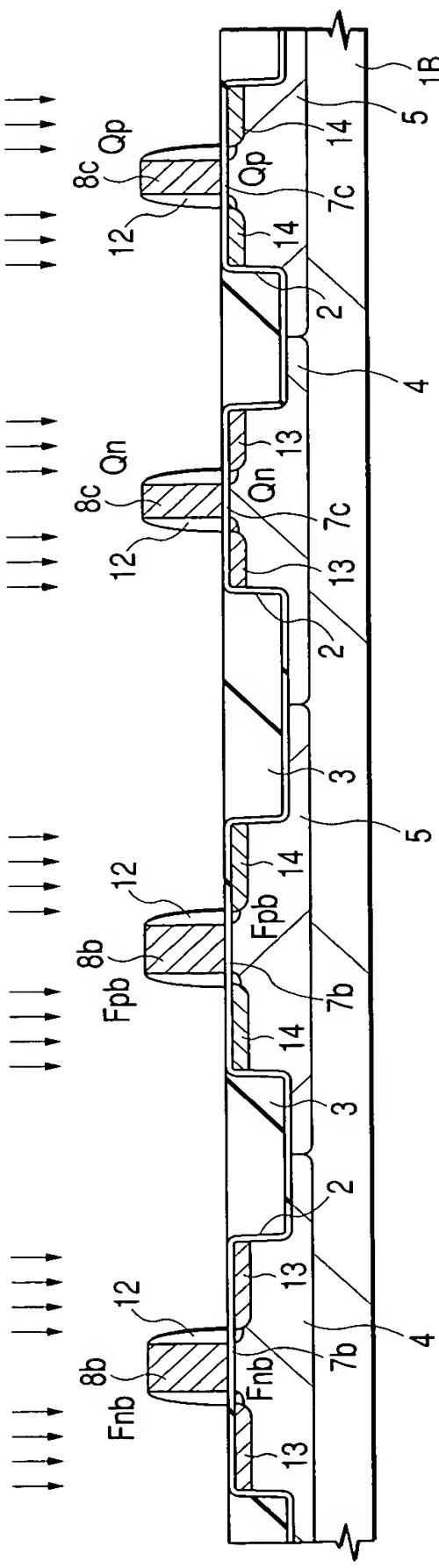


FIG. 17(b)



APPROVED	O.G. FIG.
BY	
DRAFTSMAN	SUBCLASS

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FIG. 18(a)

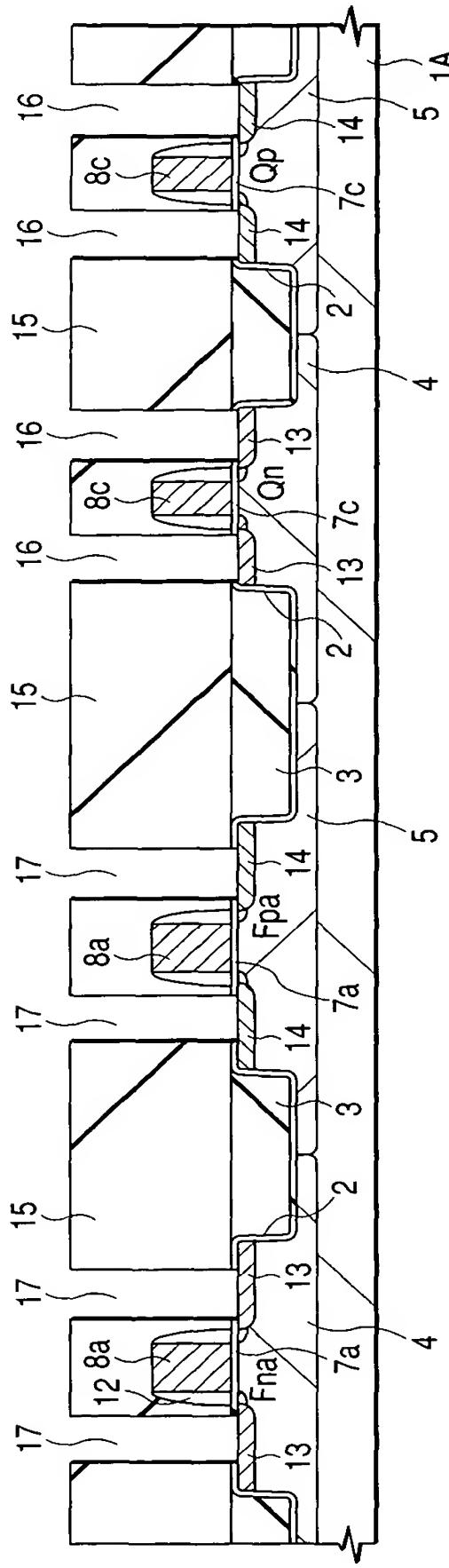


FIG. 18(b)

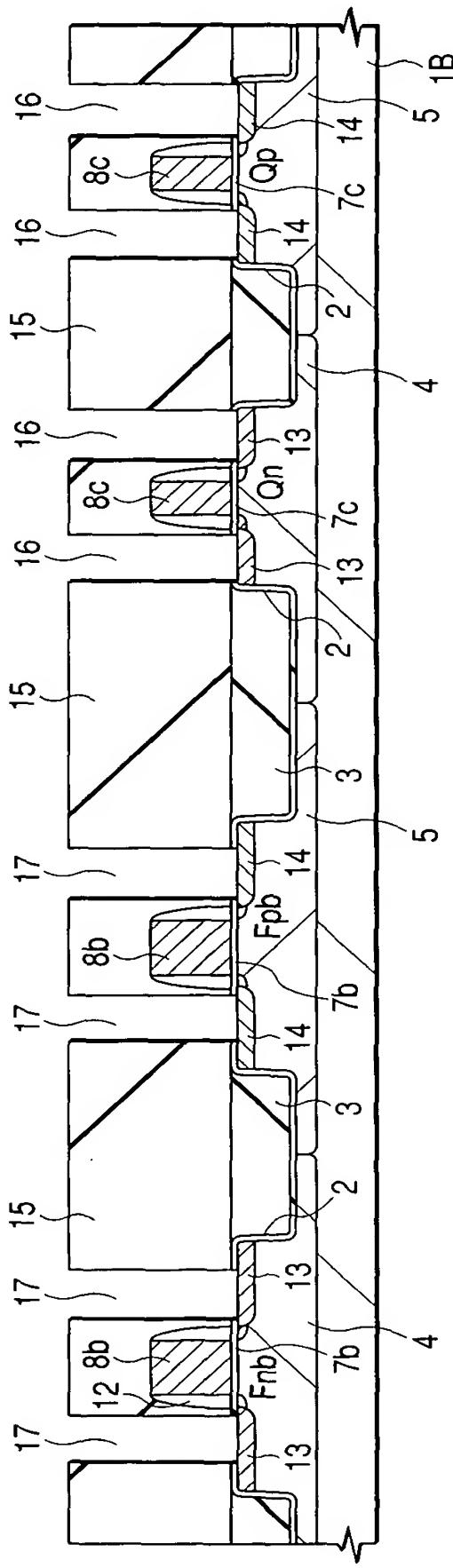


FIG. 19

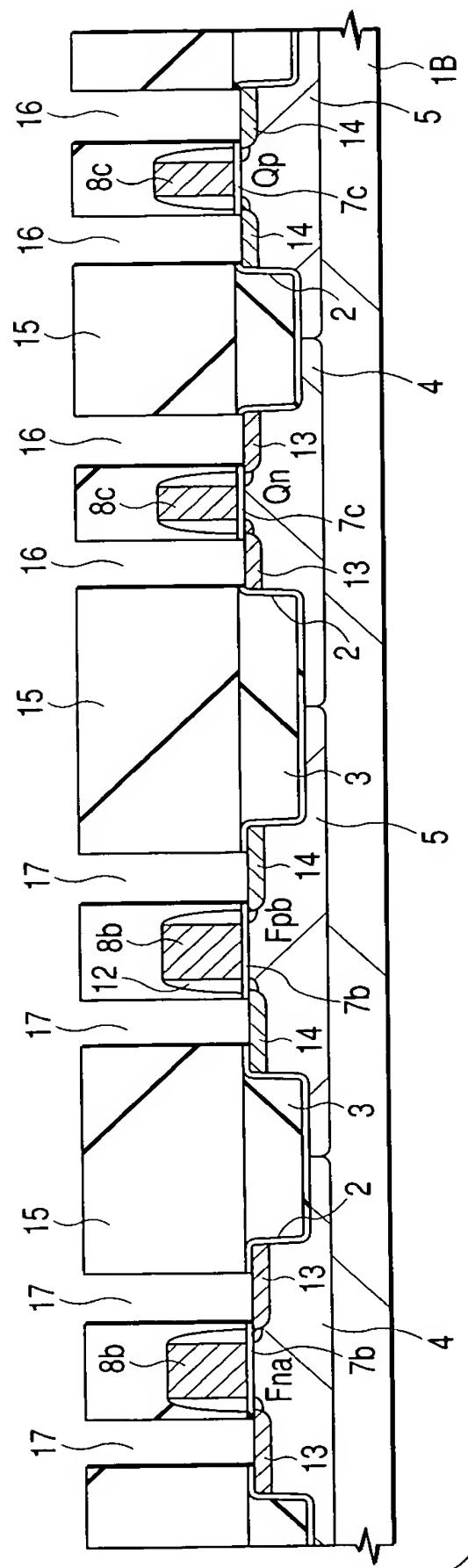
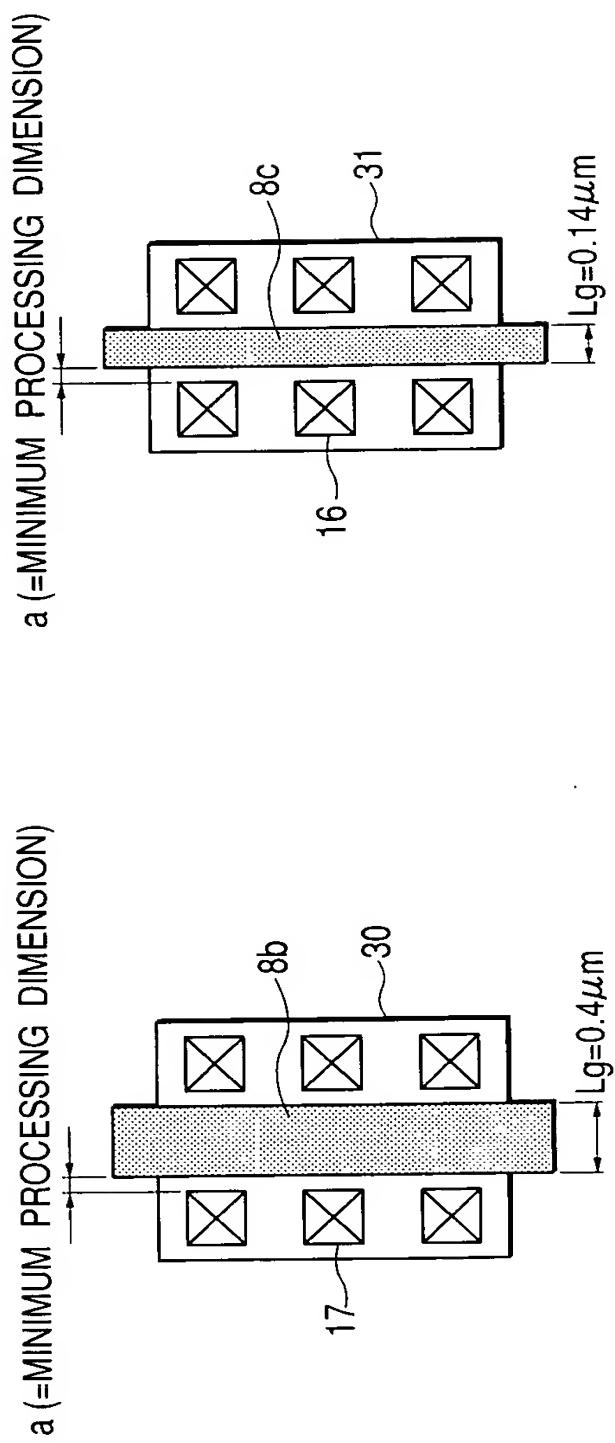


FIG. 20

a (=MINIMUM PROCESSING DIMENSION) a (=MINIMUM PROCESSING DIMENSION)

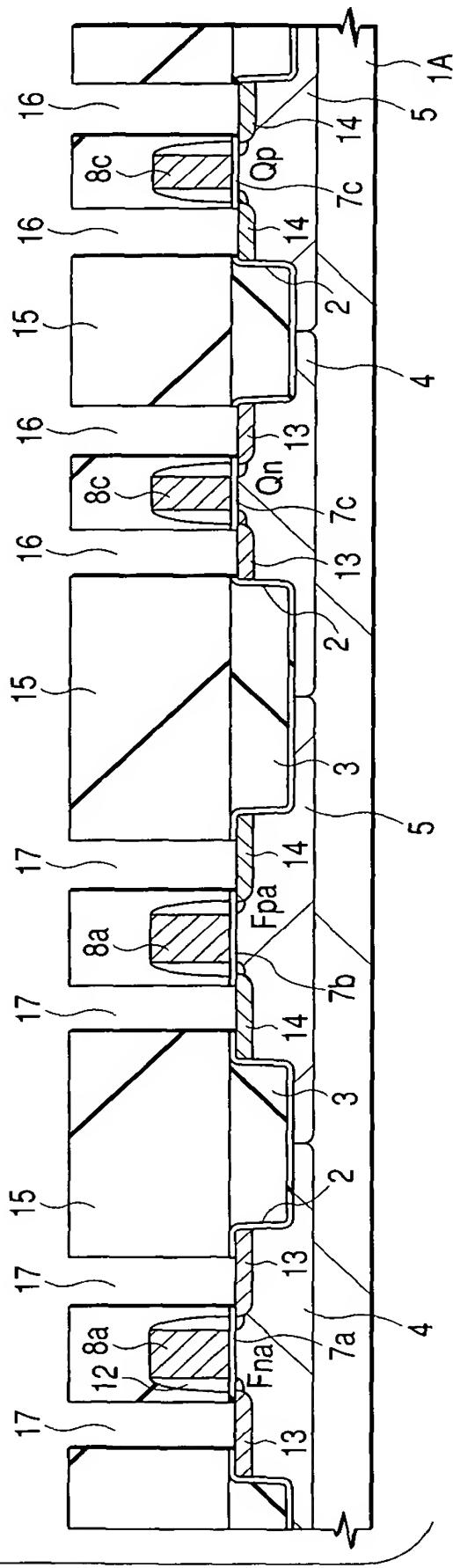
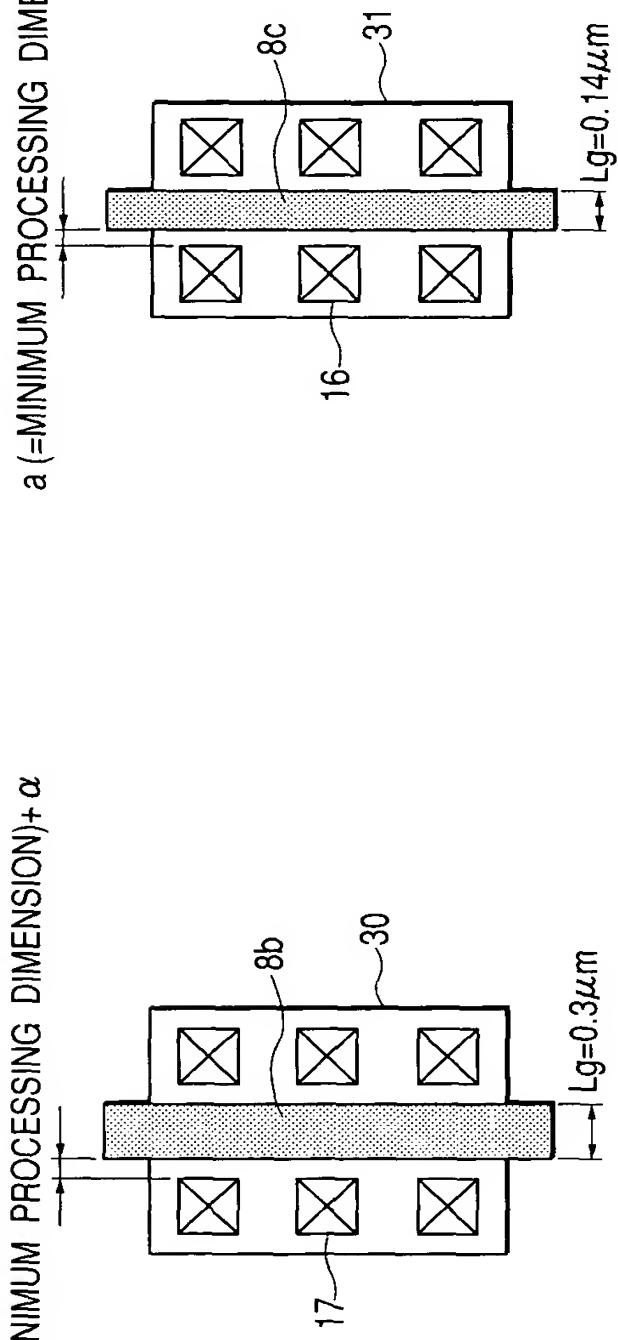
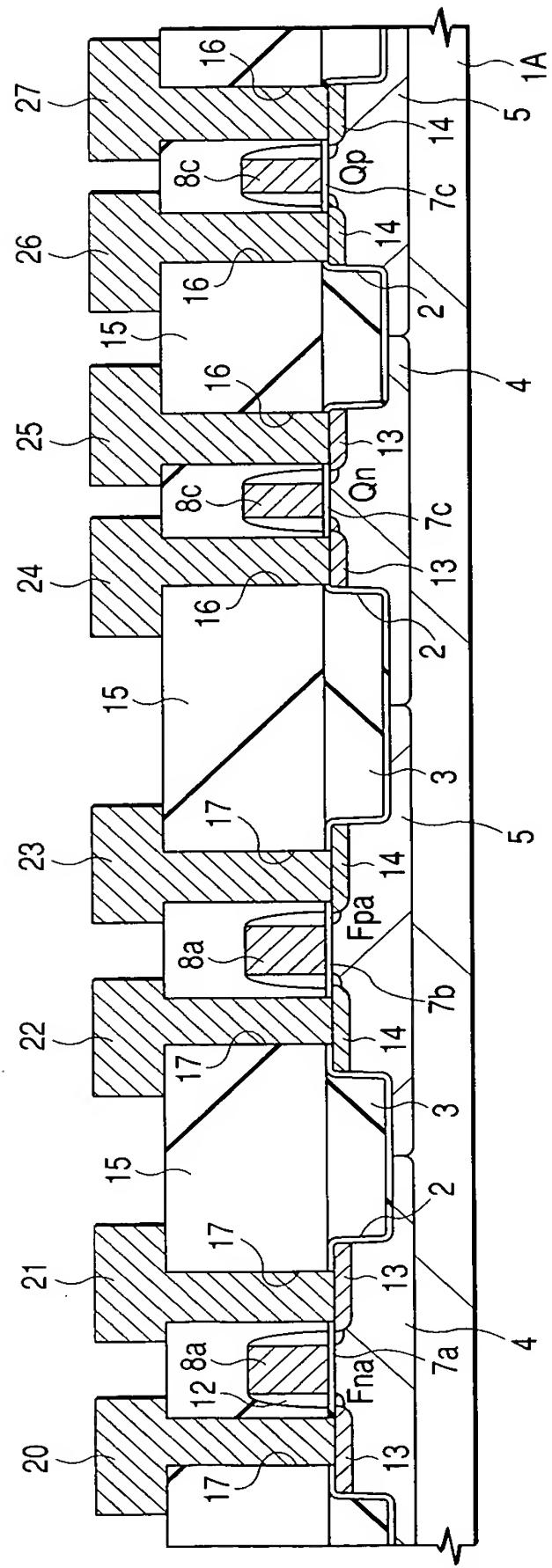


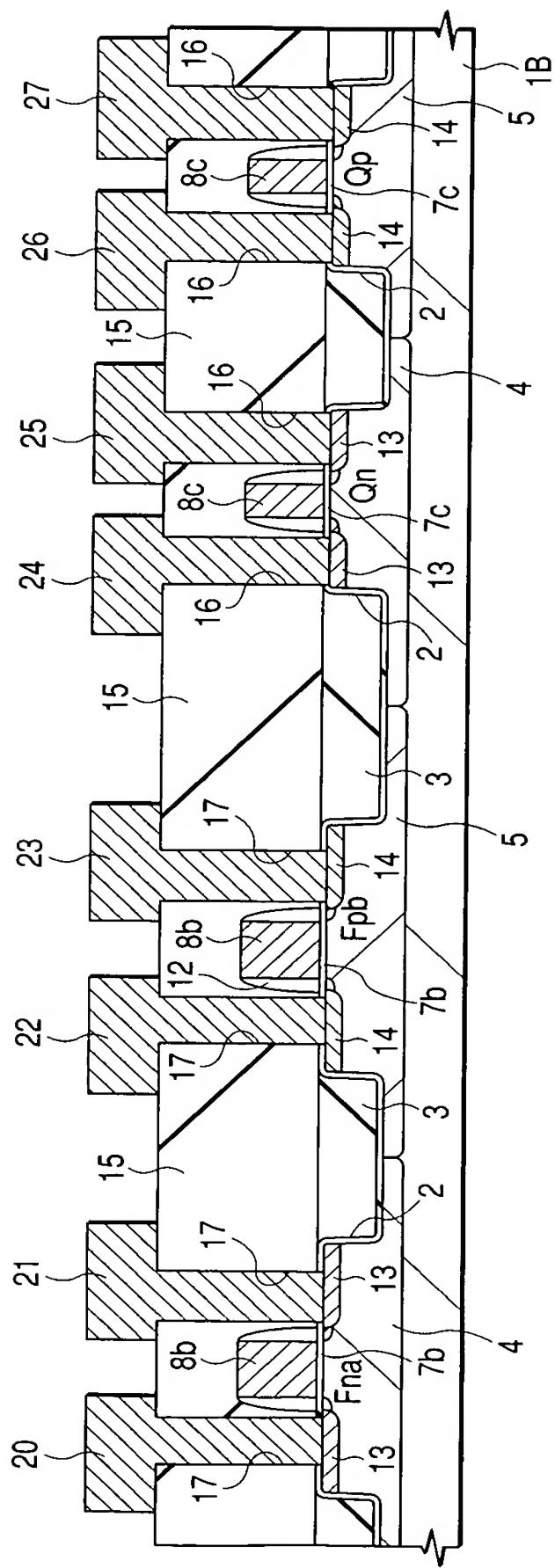
FIG. 21



APPROVED BY	O.G. FIG.
DRAFTSMAN	CLASS SUBCLASS

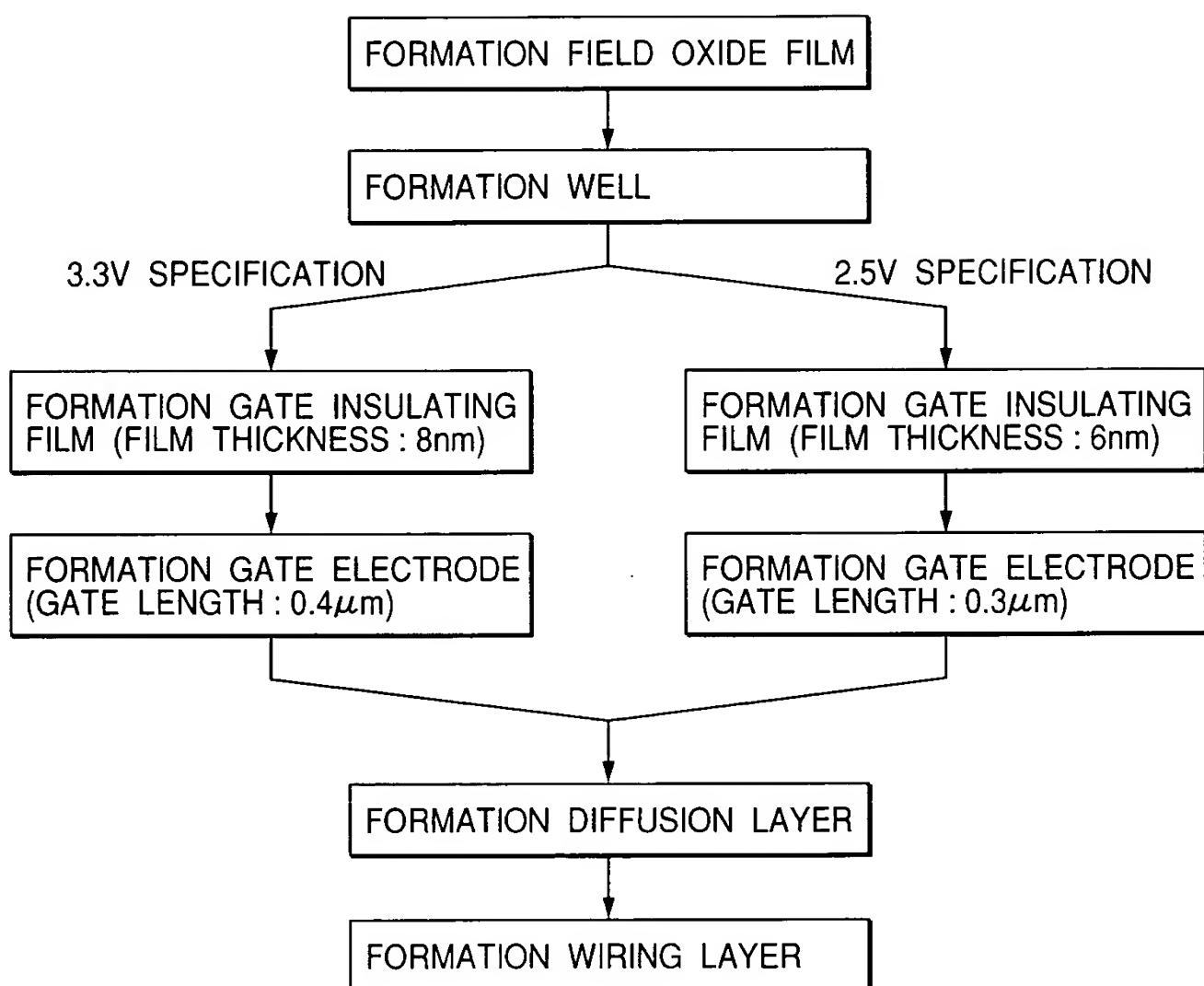
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FIG. 22



APPROVED BY	O.G. FIG.
	CLASS SUBCLASS
DRAFTSMAN	

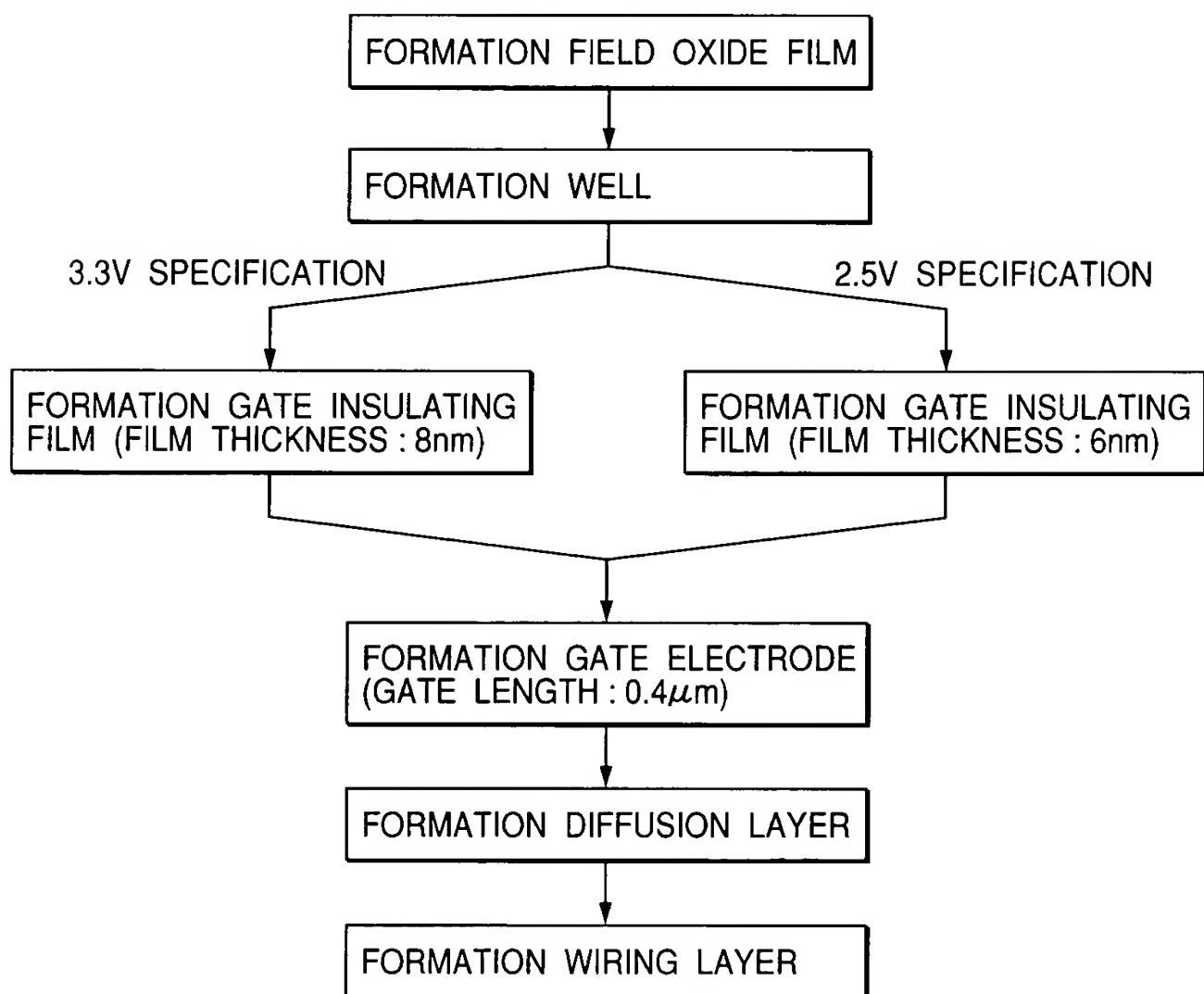
FIG. 23



APPROVED	O.G. FIG.
BY	CLASS
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FIG. 24



APPROVED	O.G. FIG.
BY	CLASS SUBCLASS
DRAFTSMAN	

FIG. 25

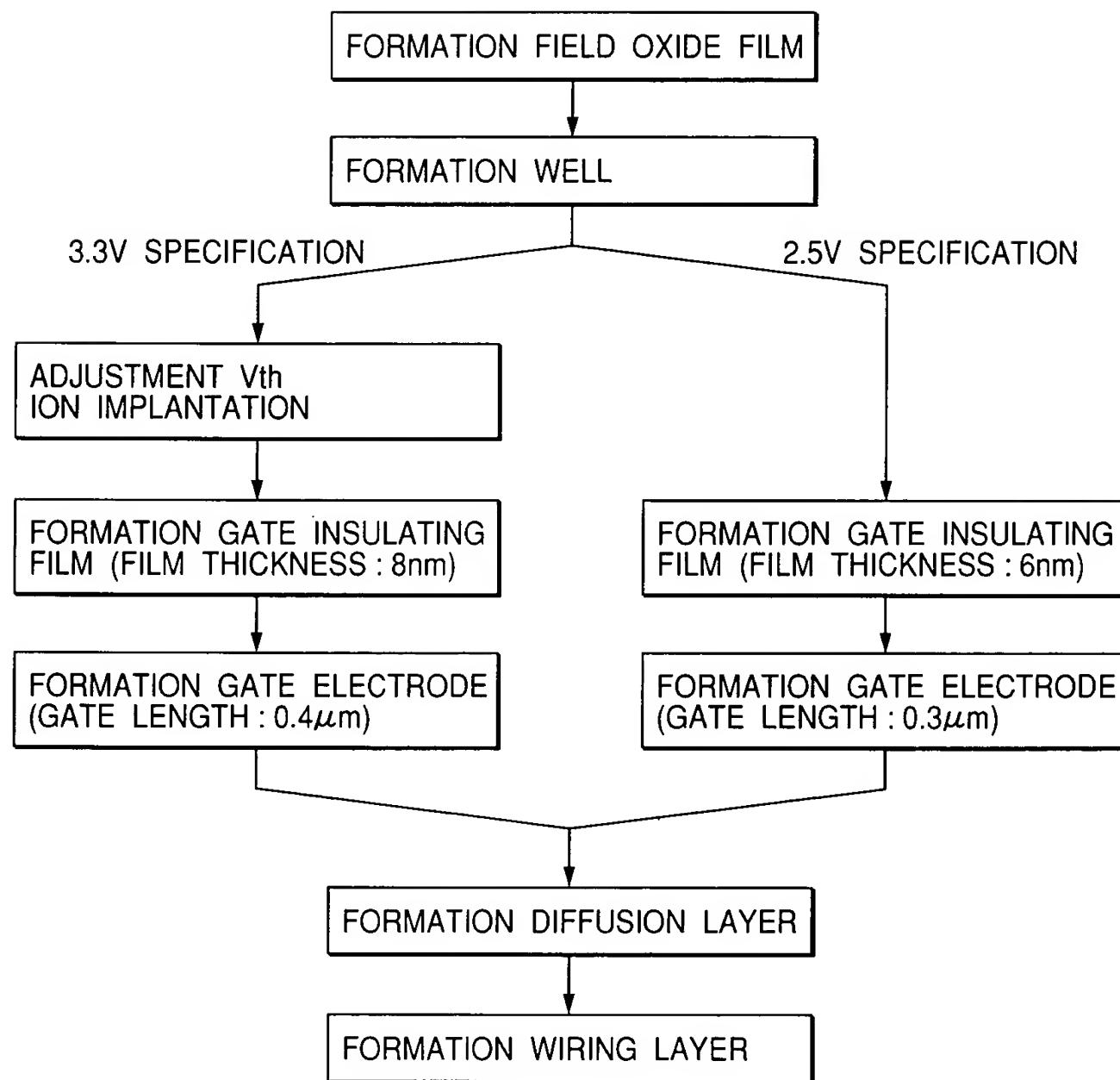
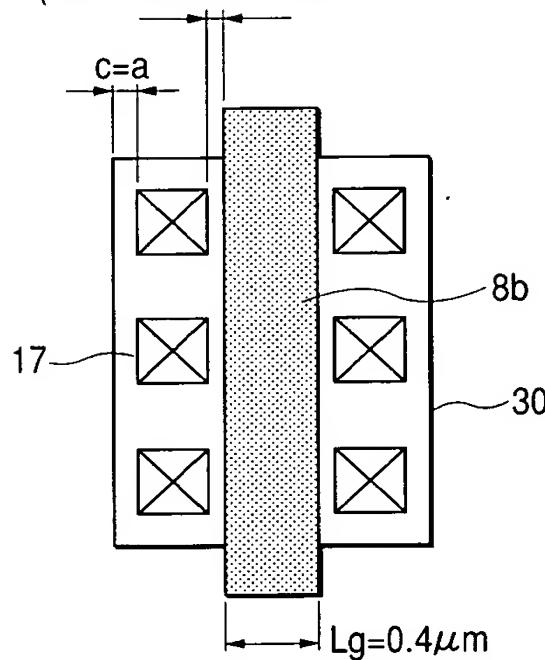


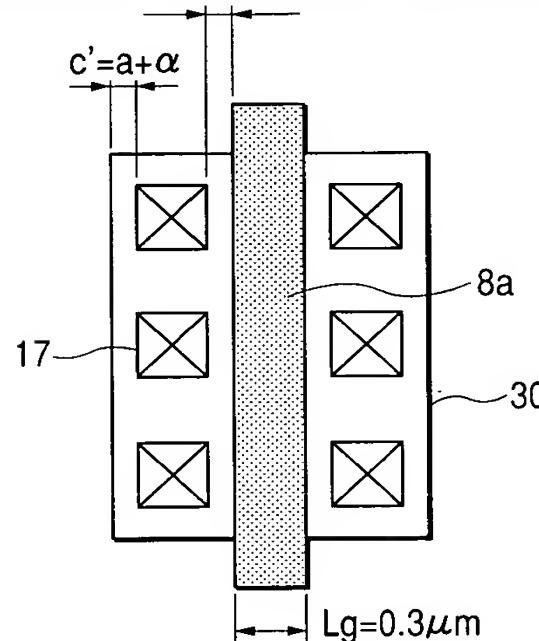
FIG. 26

a (=MINIMUM PROCESSING DIMENSION)



3.3V WITHSTANDING MOS TRANSISTOR

a (=MINIMUM PROCESSING DIMENSION)



2.5V WITHSTANDING MOS TRANSISTOR

APPROVED BY	O.G. FIG.
	CLASS
DRAFTSMAN	SUBCLASS

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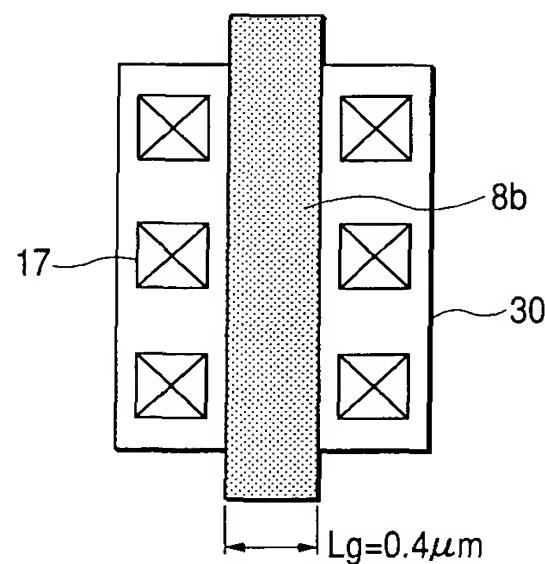
FIG. 27

SPECIFICATION	SUPPLY VOLTAGE	I/O SUPPLY VOLTAGE	INPUT SIGNAL LEVEL		SUPPLY VOLTAGE INTERNAL CIRCUIT
	VDD	VDDQ	VILmin	VIHmax	VDDI
3.3V SPECIFICATION	3.3V	3.3V	0V	VDDQ	1.5V
2.5V SPECIFICATION	2.5V	1.5V	0V	VDDQ	1.5V

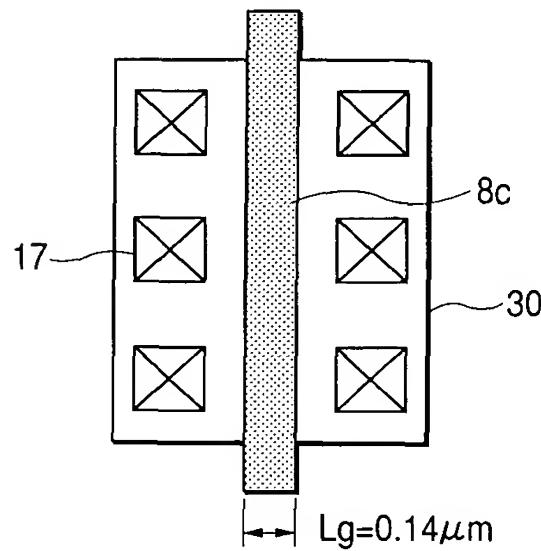
APPROVED	O.G. FIG.
BY	CLASS
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FIG. 28



3.3V WITHSTANDING MOS TRANSISTOR



2.5V WITHSTANDING MOS TRANSISTOR

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APPROVED BY	O.G. FIG.
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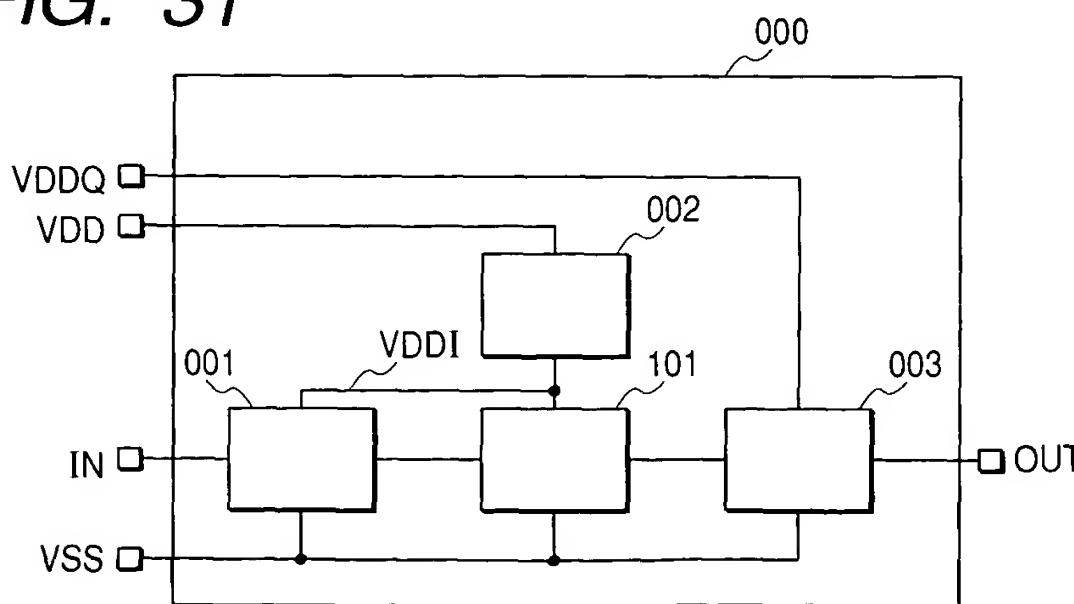
FIG. 29

SPECIFICATION	SUPPLY VOLTAGE	I/O SUPPLY VOLTAGE	INPUT SIGNAL LEVEL		SUPPLY VOLTAGE INTERNAL CIRCUIT
	VDD	VDDQ	VILmin	VIHmax	VDDI
3.3V SPECIFICATION	3.3V	3.3V	0V	VDDQ	1.5V
2.5V SPECIFICATION	2.5V	2.5V	0V	VDDQ	1.5V

FIG. 30

	GATE INSULATING FILM THICKNESS	MINIMUM PROCESSING GATE LENGTH
	TOX	Lg
3.3V WITHSTANDING MOS	8nm	0.4μm
2.5V WITHSTANDING MOS	6nm	0.3μm
1.5V WITHSTANDING MOS	3nm	0.14μm

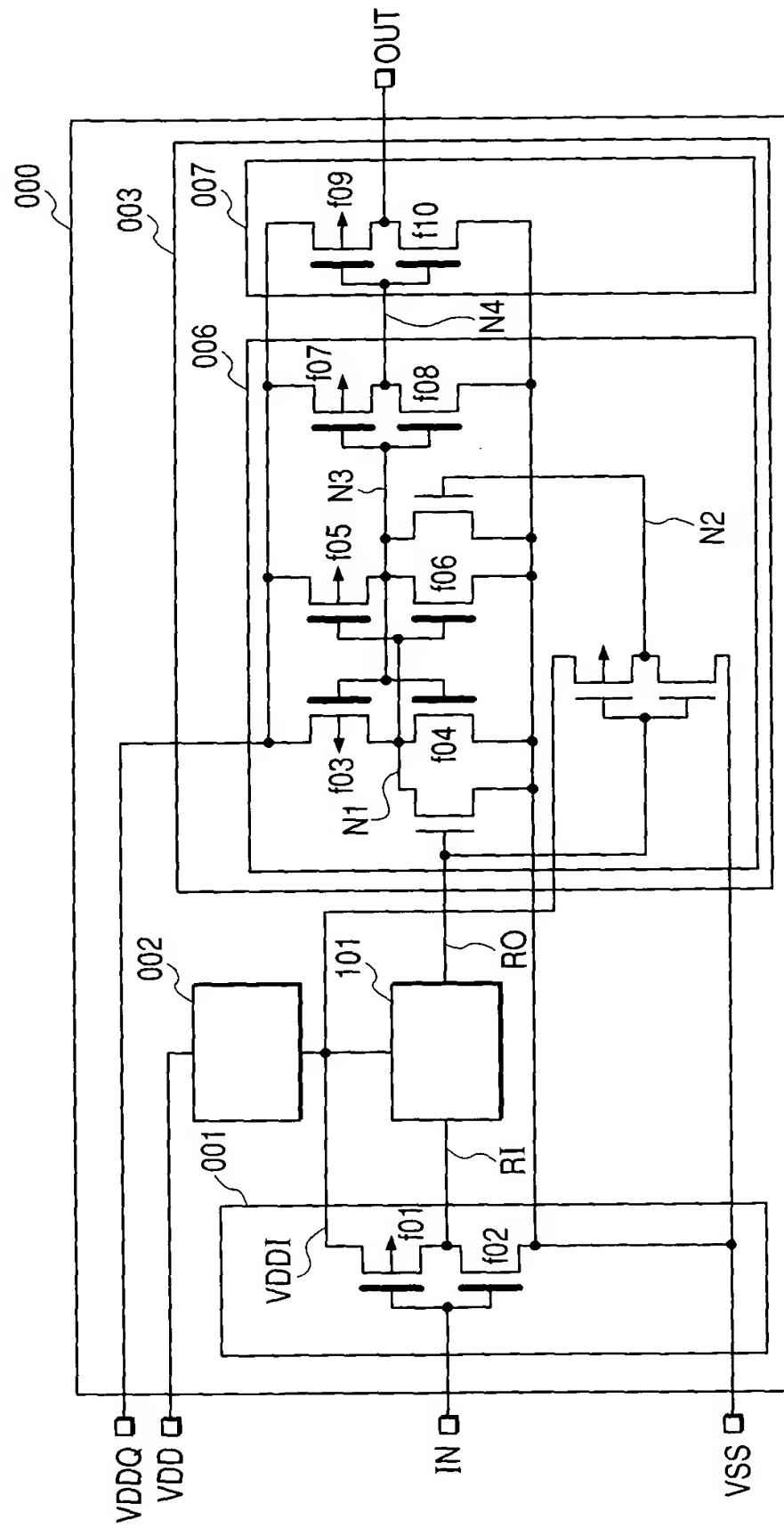
FIG. 31



APPROVED	O.G. FIG.
BY	
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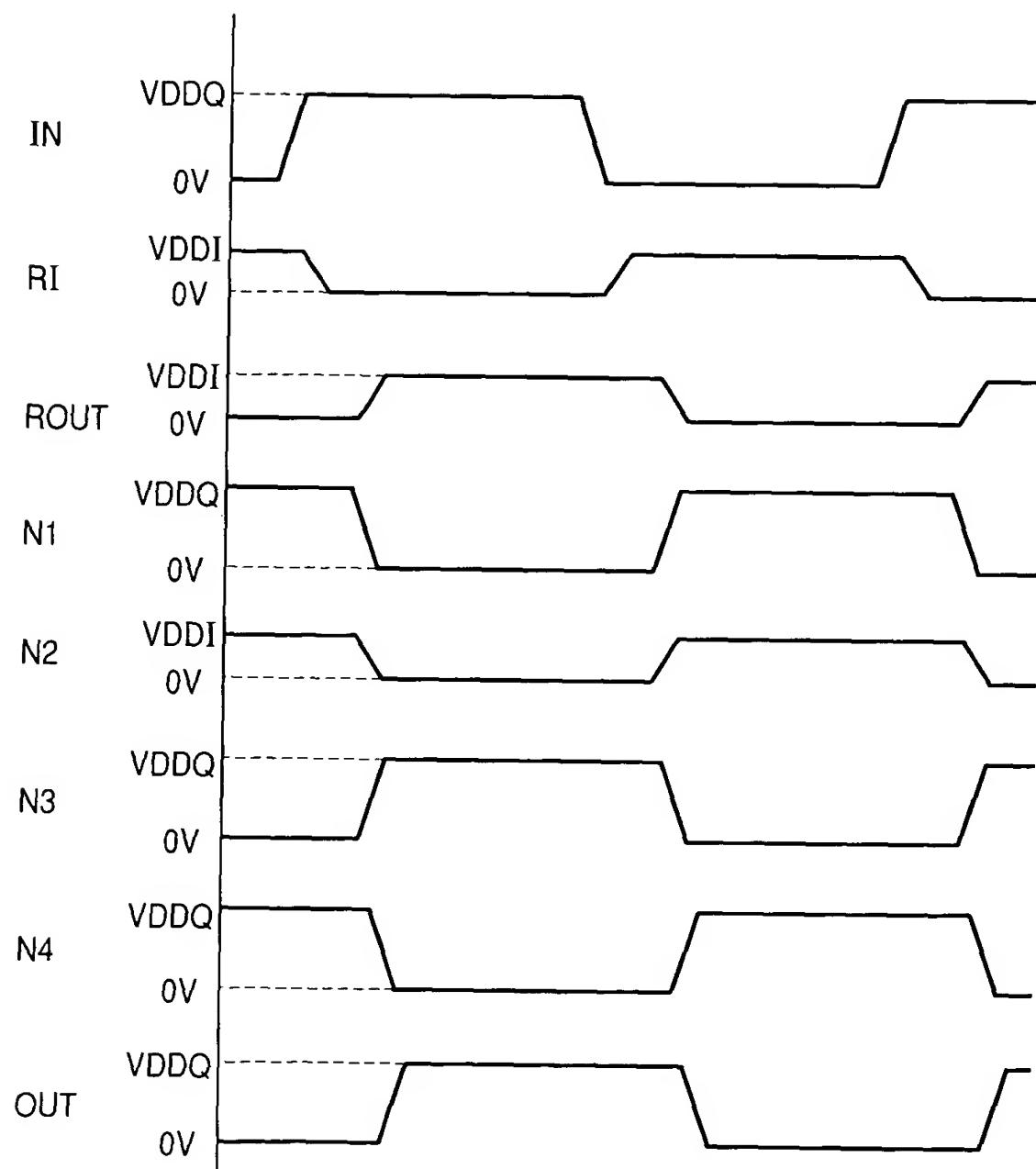
FIG. 32



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FIG. 33



APPROVED	O.G. FIG.
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FIG. 34

